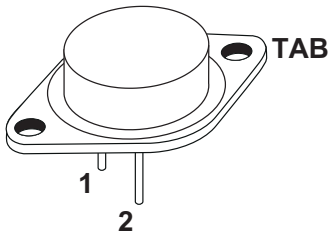
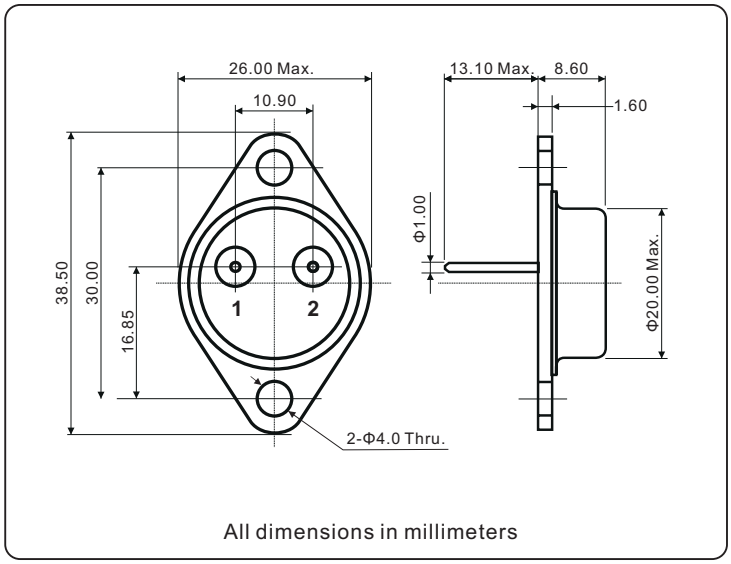
Complementary Silicon power transistors
(15A / 60V / 115W)



TO-3



FEATURES

- Designed for general designed for general-purpose switching and amplifier applications.
- DC current gain-h_{FE} = 20-70 @ I_C = 4 Adc
- Collector-Emitter saturation voltage-
  $V_{CE(sat)}$ = 1.1 Vdc (Max) @ I_C = 4 Adc
- Excellent safe operating area

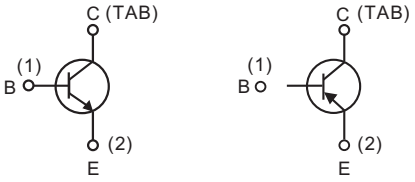
DESCRIPTION

The 2N3055 is a silicon epitaxial-base planar NPN transistor mounted in JEDEC TO-3 metal case.

It is intended for power switching circuits, series and shunt regulators, output stages and fidelity amplifiers.

The complementary PNP type is MJ2955.

INTERNAL SCHEMATIC DIAGRAM



2N3055(NPN) **MJ2955(PNP)**

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)				
SYMBOL	PARAMETER		VALUE	UNIT
V_{CBO}	Collector to base voltage (I_E = 0)		100	V
V_{CER}	Collector to emitter voltage (R_{BE} = 100Ω)		70	
V_{CEO}	Collector to emitter voltage (I_B = 0)		60	
V_{EBO}	Emitter to base voltage		7	
I_C	Collector current		15	A
I_B	Base current		7	
P_D	Total power dissipation	T_C= 25°C	115	W
	Derate above 25ºC		0.657	W/ºC
T_j	Junction temperature		200	°C
T_{stg}	Storage temperature		-65 to 200	

*For PNP types voltage and current values are negative.

THERMAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)			
SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-c)}$	Thermal resistance, junction to case	1.50	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)					
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**MAX**	**UNIT**
I_{CEX}	Collector cutoff current	V_{CE} = 100V, V_{BE} = -1.5V		1.0	mA
		V_{CE} = 100V, V_{BE} = -1.5V, T_C = 150°C		5.0	
I_{CEO}	Collector cutoff current	V_{CE} = 30V, I_B = 0		0.7	mA
I_{EBO}	Emitter cutoff current	V_{EBO} = 7V, I_C = 0		5.0	
$V_{CEO(SUS)}$*	Collector to emitter sustaining voltage	I_C = 200mA, I_B = 0	60		V
$V_{CER(SUS)}$*	Collector to emitter sustaining voltage	I_C = 200mA, R_{BE} = 100Ω	70		
V_{CBO}	Collector to base voltage	I_E = 0	100		
V_{EBO}	Emitter to base voltage	I_C = 0	7		
h_{FE}	Forward current transfer ratio (DC current gain)	I_C = 4A, V_{CE} = 4V	20	70	
		I_C = 10A, V_{CE} = 4V	5		
$V_{CE(sat)}$*	Collector to emitter saturation voltage	I_C = 4A, I_B = 400mA		1.1	V
		I_C = 10A, I_B = 3.3A		3.0	
$V_{BE(on)}$*	Base to emitter on voltage	V_{CE} = 4V		1.5	
f_T	Transition frequency	I_C = 0.5A, V_{CE} = 10V, f = 1.0MHz	2.5		MHz
$I_{s/b}$*	Second breakdown collector current with base forward baised	V_{CE} = 40V, t = 1.0s	2.87		A

*Pulsed : Pulse duration = 300 μs, duty cycle 1.5%.
*For PNP types voltage and current values are negative.

Fig.1 Power derating

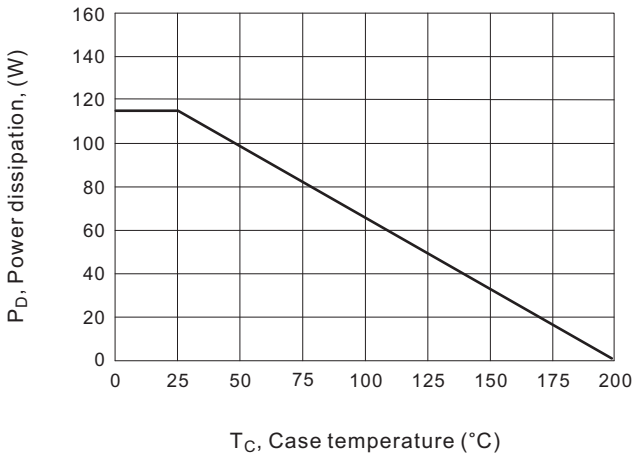
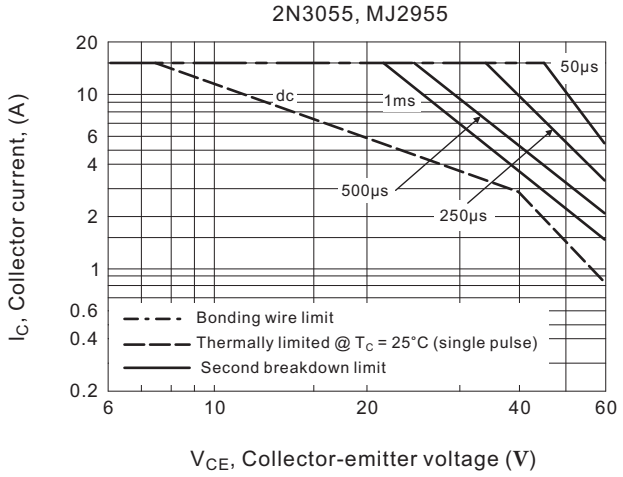


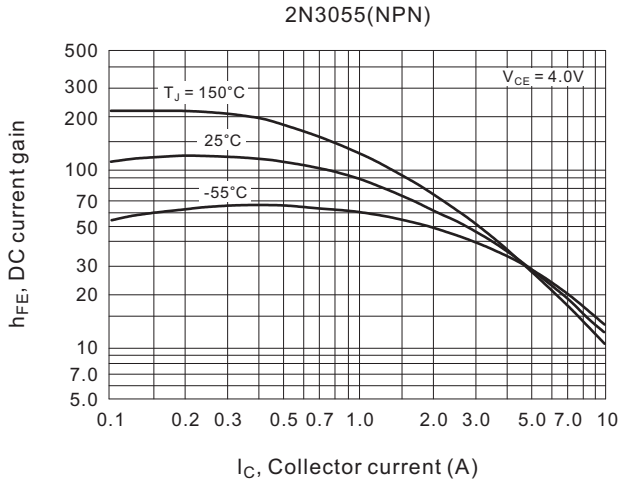
Fig.2 Active region safe operating area



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of fig.2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to fig.1

Fig.3 DC Current gain



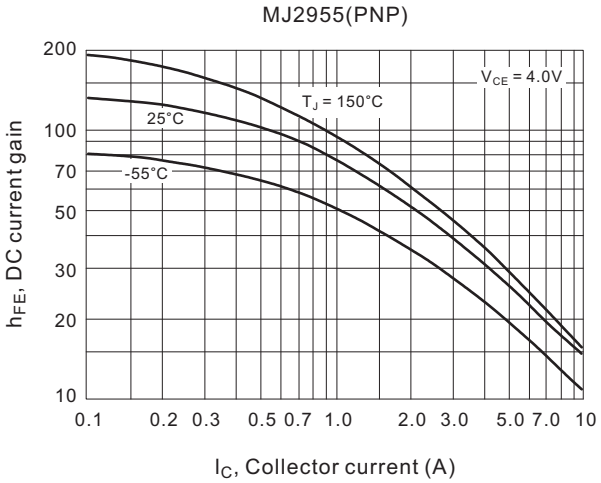
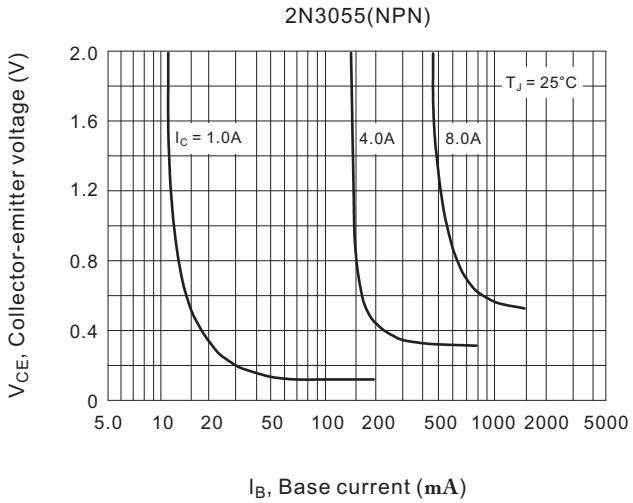


Fig.4 Collector saturation region



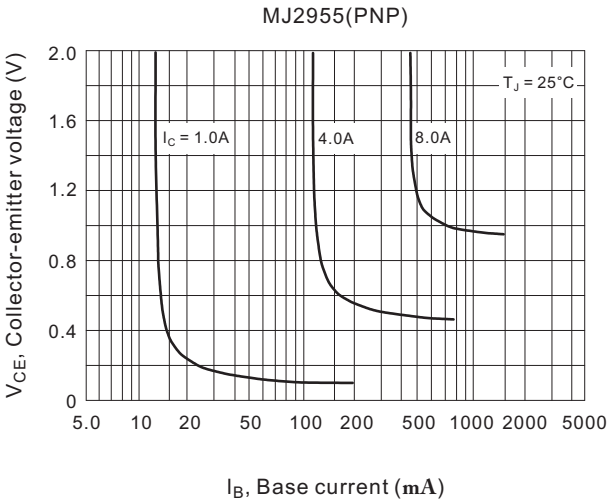
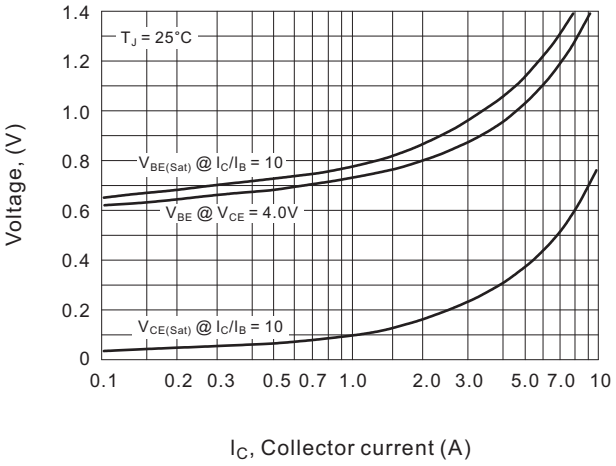


Fig.5 "On" Voltages

2N3055(NPN)



MJ2955(PNP)